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EXAMINER	
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ART UNIT	PAPER NUMBER
2192	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/633,012	WANG ET AL.	
	Examiner	Art Unit	
	Isaac T. Tecklu	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,7,9-31 and 33-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-7, 9-31 and 33-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment filed on 04/30/2007.
2. Claims 1, 7, 10, 11-12, 18, 26-31 and 33 have been amended.
3. Claims 5, 8 and 32 have been cancelled.
4. New claims 34-41 have been added.
5. Claims 1-4, 6-7, 9-31 and 33-41 have been examined.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-4, 6-7, 9-31 and 33-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Hughes et al. (US 2001/0037434 A1).

Per claim 1 (Currently Amended), Hughes discloses an apparatus comprising:

a processor including: (e.g. FIG. 12 and related text)

marking logic to mark instruction information for an instruction of a speculative thread as speculative (paragraph [0082] "... instructions speculatively fetched ...");

blocker logic to prevent data associated with a store instruction of the speculative thread from being forwarded to an instruction of a non-speculative thread (paragraph [0076] "... load

instruction may be restricted to be performed non-speculatively ..." and paragraph [0089] "... stores may be committed when they become non-speculative ..."), the blocker logic further to prevent the data from being stored in a memory system (..." paragraph [0154] "... prevented from reprobing and the store data is forwarded using dependency ...").

Per claim 2, Hughes discloses the apparatus of claim 1, wherein: blocker logic is further to allow the data associated with a store instruction of the speculative thread to be forwarded to an instruction of a second speculative thread (paragraph [0141] "... allows for forwarding of the store data ..." and paragraph [0170] "... allowing load hit to generally precede load misses ..." and paragraph [0217] "... allow initiating limited transfer of data ...").

Per claim 3, Hughes discloses the apparatus of claim 1, further comprising: a plurality of store request buffers (paragraph [0062] "... load or store request ..."), each store request buffer including a speculation identifier field (paragraph [0061] "... load/store buffer having storage locations for data and address ... buffer may comprises locations ... " and paragraph [0068] "... buffer identified by reorder buffer tags ...").

Per claim 4, Hughes discloses the apparatus of claim 1, wherein the memory system further comprises: a data cache that includes a safe-store indicator field associated with each entry of a tag array (e.g. FIG. 125, element 228 and FIG. 12, Processor 1 and related text).

Per claim 6, Hughes discloses the apparatus of claim 1, wherein blocker logic further includes:

dependence blocker logic to prevent data associated with a speculative store instruction from being forwarded to an instruction of the non-speculative thread (paragraph [0076] "... load

instruction may be restricted to be performed non-speculatively ..." and paragraph [0089] "... stores may be committed when they become non-speculative ..."); and

store blocker logic to prevent the data from being stored in a memory system (..." paragraph [0154] "... prevented from reprobing and the store data is forwarded using dependency ...").

Per claim 7, Hughes discloses the apparatus of claim 6, wherein: store blocker logic is outside the execution pipeline (e.g. FIG. 2 and related text).

Per claim 9, Hughes discloses the apparatus of claim 6, wherein: dependence blocker logic is included in an execution pipeline (e.g. FIG. 2 and related text).

Per claim 10 (Currently Amended), Hughes discloses the apparatus of claim 9, wherein: dependence blocker logic is included in a memory ordering buffer of the processor (paragraph [0061] "... load/store buffer having storage locations for data and address ... buffer may comprises locations ... " and paragraph [0068] "... buffer identified by reorder buffer tags ...").

Per claim 11 (Currently Amended), Hughes discloses a system, comprising:

a memory system that includes a memory device ~~dynamic random-access memory~~ (e.g. FIG. 25, element 204 and related text); and

a processor associated with the memory system, the processor including dependence blocker logic to prevent data associated with a store instruction of a speculative thread from being forwarded to an instruction of a non-speculative thread (paragraph [0061] "... load/store buffer having storage locations for data and address ... buffer may comprises locations ... " and paragraph [0068] "... buffer identified by reorder buffer tags ..."); ~~the processor further including store blocker logic to prevent the data from being stored in the memory system~~.

Per claim 12 (Currently Amended), Hughes discloses the system of claim 11, wherein: the processor further includes a store blocker logic to prevent the data from being stored in the memory system and marking logic to mark instruction information associated with the store

instruction as speculative (paragraph [0076] "... load instruction may be restricted to be performed non-speculatively ..." and paragraph [0089] "... stores may be committed when they become non-speculative ...").

Per claim 13, Hughes discloses the system of claim 12, wherein: the marking logic is further to associate a safe speculation domain ID with the instruction information (paragraph [0082] "... instructions speculatively fetched ...").

Per claim 14, Hughes discloses the system of claim 13, wherein: the marking logic is further to indicate a thread identifier as the speculation domain ID (paragraph [0082] "... instructions speculatively fetched ...").

Per claim 15, Hughes discloses the system of claim 12, further comprising: a store request buffer to store the speculation domain ID (paragraph [0061] "... load/store buffer having storage locations for data and address ... buffer may comprises locations ... " and paragraph [0068] "... buffer identified by reorder buffer tags ...").

Per claim 16, Hughes discloses the system of claim 11, wherein: the processor includes a first logical processor to execute the non-speculative thread; and the processor includes a second logical processor to execute the speculative thread (e.g. FIG. 1 and related text).

Per claim 17, Hughes discloses the system of claim 11, further comprising: a second processor that includes said dependence blocker logic and said store blocker logic; wherein said processor is to execute the non-speculative thread and said second processor is to execute the speculative thread (e.g. FIG. 1 and related text).

Per claim 18 (Currently Amended), Hughes discloses the system of claim of claim 11, wherein: the memory system includes store blocker logic to prevent the data from being stored in the memory system and a cache organized to include a plurality of tag lines, wherein each tag line of the cache includes a unique helper thread ID field (paragraph [0076] "... load

instruction may be restricted to be performed non-speculatively ..." and paragraph [0089] "... stores may be committed when they become non-speculative ...").

Per claim 19, Hughes discloses the system of claim 11, wherein: the memory system includes a cache organized to include a plurality of tag lines, wherein each tag line of the cache includes a safe-store indicator field (paragraph [0076] "... load instruction may be restricted to be performed non-speculatively ..." and paragraph [0089] "... stores may be committed when they become non-speculative ...").

Per claim 20, Hughes discloses the system of claim 11, wherein: the memory system includes a victim tag cache to indicate evicted cache lines that include speculative load data (e.g. FIG. 1 and related text).

Per claim 21, Hughes discloses a method, comprising:

receiving instruction information for a load instruction, the instruction information including a load address (e.g. FIG. 20 and related text);

performing a dependence check, wherein performing the dependence check includes:

determining if a store address of an in-flight store instruction matches the load address (e.g. FIG. 20 and related text); and

determining if the load instruction and the in-flight store instruction each originate with a speculative thread; forwarding, if the dependence check is successful, store data associated with the in-flight store instruction to the load instruction (e.g. FIG. 15 and related text); and

declining to forward, if the dependence check is not successful, the store data to the load instruction (paragraph [0076] "... load instruction may be restricted to be performed non-speculatively ..." and paragraph [0089] "... stores may be committed when they become non-speculative ...").

Per claim 22, Hughes discloses the method of claim 21, wherein performing the dependence check further comprises: determining if the in-flight store instruction and the load instruction originate from the same thread (e.g. FIG. 20, step 302 and related text).

Per claim 23, Hughes discloses the method of claim 22, wherein determining if the in-flight store instruction and the load instruction originate from the same thread further comprises: determining if a thread ID associated with the in-flight store instruction matches a thread ID associated with the load instruction (paragraph [0079]).

Per claim 24, Hughes discloses the method of claim 21, wherein performing the dependence check further comprises: if the load instruction and the in-flight store instruction do not each originate with a speculative thread, determining if the load instruction and the in-flight store instruction each originate with a non-speculative thread (paragraph [0182]).

Per claim 25, Hughes discloses the method of claim 21, further wherein: declining to forward further comprises declining to forward the store data to the load instruction if (the load instruction and the in-flight store instruction each originate with a speculative thread) and (the in-flight store instruction originates with a speculative thread that is not older in program order than the speculative thread from which the load instruction originates) (paragraph [0076] "... load instruction may be restricted to be performed non-speculatively ..." and paragraph [0089] "... stores may be committed when they become non-speculative ...").

Per claim 26 (Currently Amended), Hughes discloses a method, comprising:

~~processing a speculative thread cache read request;~~

in response to determining a cache line corresponding to a speculative thread (paragraph [00171] "... cache line ...");

cache write request includes dirty non-speculative data (paragraph [0222] "... write access to cache line ...");

generating a write back of the dirty non-speculative data (paragraph [0225]);

generating a write back of the dirty non-speculative data (paragraph [0122] "... non speculative bit ..."); and

marking the cache line as speculative (paragraph [0186] "... stores and marks ...")

processing a speculative thread cache write request; and processing a cache access request from a non-speculative thread (paragraph [0156] "... speculative state of processor ...").

Per claim 27 (Currently Amended), Hughes discloses the method of claim 26, ~~wherein processing a speculative thread cache read request~~ further comprising ~~comprises~~: forwarding speculative data from a cache to the ~~a~~ speculative thread responsive to a data speculative thread cache read request (paragraph [0156] "... speculative state of processor ...")

Per claim 28 (Currently Amended), Hughes discloses the method of claim 26, ~~wherein processing a speculative thread cache read request~~ comprising ~~comprises~~: forwarding non-speculative store data from the ~~a~~ cache to a speculative thread responsive to a data speculative thread cache read request (paragraph [0156] "... speculative state of processor ...").

Per claim 29 (Currently Amended), Hughes discloses the method of claim 26, ~~wherein processing a speculative thread cache read request~~ further comprising ~~comprises~~: forwarding non-speculative store data from the ~~a~~ cache to a speculative thread responsive to a data speculative thread cache read request (paragraph [0156] "... speculative state of processor ...")

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Per claim 30 (Currently Amended), Hughes discloses the method of claim 26, further comprising processing a cache access request from a non-speculative thread, wherein processing a cache access request from a non-speculative thread ~~further~~ comprises: if a cache does not include a cache line associated with the cache access request, allocating a new cache line (paragraph [0076] "... load instruction may be restricted to be performed non-speculatively ..." and paragraph [0089] "... stores may be committed when they become non-speculative ...");

wherein allocating a new cache line further comprises: if the new cache line includes dirty speculative data, allocating the new cache line without generating a writeback operation (paragraph [0122] "... non speculative bit ..."; and if the new cache line includes dirty non-

speculative data, generating a writeback operation (paragraph [0156] "... speculative state of processor ...").

Per claim 31 (Currently Amended), Hughes discloses the method of claim 26, ~~wherein processing a speculative thread cache read request~~ further comprising ~~comprises~~: allowing the speculative thread to write data to the cache if the ~~a~~ cache line corresponding to the speculative thread cache write request includes speculative data (paragraph [0076] "... load instruction may be restricted to be performed non-speculatively ..." and paragraph [0089] "... stores may be committed when they become non-speculative ...").

Per claim 33 (Currently Amended), Hughes discloses the method of claim 26, ~~wherein processing a speculative thread cache read request~~ further comprising ~~comprises~~:

if the cache does not contain data in a cache line corresponding to the speculative thread cache write request ~~data cache address~~:

allocating a new cache line (paragraph [00171] "... cache line ...");

marking the new cache line as speculative (paragraph [0082] "... instructions speculatively fetched ..."); and

allowing the speculative thread to write speculative data to the new cache line (paragraph [0076] "... load instruction may be restricted to be performed non-speculatively ..." and paragraph [0089] "... stores may be committed when they become non-speculative ...").

Per claim 34 (New), Hughes discloses an apparatus comprising:

a processor including (e.g. FIG. 1 and related text):

a first logical processor to execute a speculative thread (paragraph [0165] "... speculative state of processor ..." and e.g. FIG. 1 and related text);

a second logical processor to execute a non-speculative thread (paragraph [0128] "... non executing speculatively ..." and e.g. FIG. 1 and related text);

a storage area to include a speculation identifier (ID) field, the speculation ID field to hold a first value to indicate an associated store instruction is associated with the speculative thread (paragraph [0056] ".. buffer tag identifying ..." and e.g. FIG. 1 and related text); and

control logic to prevent data associated with the store instruction from being consumed by the non-speculative thread, based on the speculation ID holding the first value (paragraph [0076] "... load instruction may be restricted to be performed non-speculatively ..." and paragraph [0089] "... stores may be committed when they become non-speculative ...").

Per claim 35 (New), Hughes discloses the apparatus of claim 34, wherein: the first and the second logical processors are the same logical processor, and wherein the non-speculative thread and the speculative thread are to be time multiplexed for execution on the same logical processor (paragraph [0078] "... multiplexer ...").

Per claim 36 (New), Hughes discloses the apparatus of claim 34, wherein: the storage area includes a store buffer, and wherein the speculation ID field is included within a store buffer entry of the store buffer, the store buffer entry to also hold a first address associated with the store instruction and the data associated with the store instruction (paragraph [0056] ".. buffer tag identifying ..." and e.g. FIG. 1 and related text).

Per claim 37 (New), Hughes discloses the apparatus of claim 36, wherein: the first value is to include a first identifier (ID) value associated with the first logical processor (paragraph [0056] ".. buffer tag identifying ..." and e.g. FIG. 1 and related text).

Per claim 38 (New), Hughes discloses the apparatus of claim 37, wherein: the control logic includes comparison logic to compare a second address and a second ID value, which are associated with a load Instruction that is to be executed as part of the non-speculative thread on

the second logical processor, with the first address and the first ID value (paragraph [0056] ".. buffer tag identifying ..." and e.g. FIG. 1 and related text); and

store blocker logic to prevent data associated with the store instruction from being consumed by the load instruction that is to be executed as part of the non-speculative thread, in response to the first ID value and the first address not matching the second ID value and the second address (paragraph [0076] "... load instruction may be restricted to be performed non-speculatively ..." and paragraph [0089] "... stores may be committed when they become non-speculative ...").

Per claim 39 (New) , Hughes discloses the apparatus of claim 34, wherein: the processor further includes a third logical processor to execute an additional speculative thread, and wherein the control logic is to allow data associated with the store instruction from being consumed by the additional speculative thread (paragraph [0141] "... allows for forwarding of the store data ..." and paragraph [0170] "... allowing load hit to generally precede load misses ..." and paragraph [0217] "... allow initiating limited transfer of data ...").

Per claim 40 (New), Hughes discloses the apparatus of claim 34, wherein: the first value is to include a 1-bit mode value comparison logic (paragraph [0079] "... compared to the total ...").

Per claim 41 (New), Hughes discloses the apparatus of claim 34, wherein: the processor further includes marking logic to set the speculation ID field to the first value in response to detecting the store instruction associated with the speculative thread (paragraph [0082] "... instructions speculatively fetched ...").

Response to Arguments

8. Applicant's arguments with respect to claims 1-4, 6-7, 9-31 and 33-41 have been considered but are moot in view of the new ground(s) of rejection. See Hughes art made of record.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Isaac T. Tecklu whose telephone number is (571) 272-7957. The examiner can normally be reached on M-TH 9:300A - 8:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TUAN DAM
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